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EXAMINER	
SZETO, JACK W	

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,432	DUNSTAN, ROBERT A.	
	Examiner	Art Unit	
	Jack W. Szeto	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-35* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Nov. 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Official Action

Status of the Specification and Claims

Claims 1, 4, 6-10, 14, 16-23, 28-29, and 32-35 are rejected under 102(e).

Claims 2, 3, 11-13, 15, 24-27, and 30-31 are rejected under 103(a).

Claim 5 is objected to as being dependent upon rejected base claims but contain allowable subject matter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4, 6-10, 14, 16-23, 28-29, and 32-35 are rejected under 35 U.S.C. 102(e) as being anticipated by Westerinen (United States Patent Publication No. 2004/0088589).

As per claim 1, Westerinen discloses:

In an apparatus, a method of operation comprising:

in response to an AC failure condition of the apparatus, supplying power from a backup power source to the apparatus for at least a time period [para 0024: battery sustain operation of computer for a period of time];

additionally initiating a suspend process to place the apparatus in a suspended to memory state, to be sustained by the supplied backup power [Figure 4: system in place in state S3 (suspended to memory) following a power failure and sustained by a battery (reference 96)]; and

intervening and preserving a persistent copy of an operational state of the apparatus, before completing the suspend process and placing the apparatus in the suspended to memory state, sustained by the supplied backup power [para 0024: before entering hibernation the contents of the RAM and CPU settings (operational state) are transferred to a hard disk with on battery power].

As per claim 4, Westerinen discloses:

The method of claim 1, wherein

the intervening comprises transferring control to an input/output system (BIOS) of the apparatus [para 0015: BIOS is programmed to be part of the mechanism for preserving the data state]; and

the preserving comprises the BIOS saving the operational state of the apparatus to a persistent storage [para 0015: BIOS is programmed to be part of the mechanism for preserving the data state].

As per claim 6, Westerinen discloses:

The method of claim 1, wherein the method further comprises

monitoring for absence of AC to a power supply of the apparatus [para 0026: switchover circuit monitor for power failure]; and

generating a signal indicating AC failure on detection of absence of AC to the power supply [para 0027: signals generated by switchover circuit].

As per claim 7, Westerinen discloses:

The method of claim 6, wherein the monitoring and generating are performed by the power supply [Figure 3, reference 76: switchover circuit within power supply].

As per claim 8, Westerinen discloses:

In an apparatus, a method of operation comprising:

maintaining the apparatus in a suspended to memory state, employing a backup power source, while the apparatus is in an AC failed condition, resulting in a memory of the apparatus having a suspended operational state of the apparatus [para 0024: the system saves the operational states in memory while being powered by a battery when AC power has failed];

monitoring for re-application of AC to the apparatus while the apparatus is in the suspended to memory state maintained by the backup power source [para 0034: monitors for steady AC re-application while system is in hibernation]; and

resuming the apparatus to an active state on re-application of AC to the apparatus, where the apparatus continues operation, starting from the operational state previously suspended in the memory [para 0034: resumes working state using the previously stored state data].

As per claim 9, Westerinen discloses:

The method of claim 8, wherein

the method further comprises signaling a controller of the apparatus on re-application of AC to the apparatus while the apparatus is in the suspended to memory state [para 0034: controller waits for AC re-application];

handling the signaling by the controller as a device wake event, causing a basic input/output system (BIOS) of the apparatus to gain control [para 0015 & para 0032: BIOS handles resume process after controller handles the wake-up event]; and

the BIOS initiating a resume process, and transferring control to an operating system (OS) of the apparatus to complete the resume process, transition the apparatus from the suspended to memory state to the active state, and continue operation of the apparatus, starting from the previous suspended operational state in memory [para 0024: BIOS resumes same condition of system before hibernation and passes control to the OS after initialization (as per para 0015)]

As per claim 10, Westerinen discloses:

The method of claim 9, wherein the signaling of the controller is performed by a power supply of the apparatus [Figure 3, reference 76: switchover circuit within power supply].

As per claim 14, Westerinen discloses:

A system comprising:

a memory to store at least a current operational state of the system [Figure 3, reference 17: state data];

a persistent storage [Figure 3, reference 23];

a basic I/O system (BIOS) operatively coupled the memory and the persistent storage [Figure 3, reference 26], to intervene and save a persistent copy of the operational state of the system in the persistent storage [para 0015: BIOS involved with preserving state data], when a suspend process is initiated by an operating system (OS) to place the system in the suspended to memory state [para 0029: OS starts the hibernation (suspend process)]; and

a controller operatively coupled to the OS [Figure 3: Controller coupled to OS] to cause the OS to initiate the suspend process to place the system in the suspended to memory state, when the system is in an AC failed condition [para 0029: OS starts the hibernation (suspend process) after alarm is sent via the register in controller];

As per claim 16, Westerinen discloses:

The system of claim 14, wherein the system further comprises a power supply coupled to at least the controller, to monitor for presence of AC, and generate a signal indicating AC failure on detection of absence of AC [Figure 4, and para 0027: signals generated by switchover circuit].

As per claim 17, Westerinen discloses:

The system of claim 14, wherein the system further comprises a power supply including a backup power source, coupled to the memory, to source power to the memory to sustain the suspended to memory state for at least a time period during the AC failed condition [Figure 3,

reference 76: battery, ac source and coupled to memory to power it].

As per claim 18, Westerinen discloses:

The system of claim 14, wherein the controller is equipped to cause the OS to initiate the suspend process to place the system in the suspended to memory state, when the system is in an AC failed condition, by way of an interrupt when the system is in an active state [para 0024: before entering hibernation (suspend to memory state) the contents of the RAM and CPU settings (operational state) are transferred to a hard disk].

As per claim 19, Westerinen discloses:

The system of claim 14, wherein the controller is equipped to cause the OS to initiate the suspend process to place the system in the suspended to memory state [Figure 4 and para 0029: OS places the system in suspend to memory state after alarm is sent via the register in controller], when the system is in an AC failed condition [Figure 4, reference 92 to reference 96: AC power failure], by waking the system when the system is in a suspended to memory state [Figure 4, reference 96 to 98: controller wakes up system].

As per claim 20, Westerinen discloses:

The system of claim 14, wherein the system further comprises a networking interface operatively coupled to the BIOS [Figure 3, reference 26].

As per claim 21, Westerinen discloses:

A system comprising:

a memory to store an operational state of the system [Figure 3, reference 17: contains operational state data];

a power supply coupled to the memory, including a backup power source to sustain the memory for at least a time period, while the system is suspended to memory under an AC failure condition [Figure 3 and para 0024: battery sustain system for a while when AC fails];

a basic input/output system (BIOS) operatively coupled to an operating system (OS), and equipped to initiate a resume process and transfer to the OS to continue and complete the resume process, and place the system in an active state, where the system continues operation, starting from the previously suspended operational state of the system in memory [para 0024: BIOS resumes same condition of system before hibernation and passes control to the OS after initialization (as per para 0015)]; and

a controller operatively coupled to the BIOS to cause the BIOS to initiate the resume process on re-application of AC to the system [para 0034: controller wakes the system and the system resumes the working state by restoring the saved states (BIOS handles the restoration of states as per para 0024)].

As per claim 22, Westerinen discloses:

The system of claim 21, wherein the power supply is further equipped to signal the controller on re-application of AC to the system [Figure 3, reference 76: switchover circuit within power supply];

the controller is equipped to handle the signaling as a device wake event, causing BIOS to gain control [para 0024: BIOS resumes same condition of system before hibernation after wake up event]; and

the BIOS is equipped to initiate the resume process, upon gaining control [para 0015: BIOS handles resume process].

As per claim 23, Westerinen discloses:

The system of claim 21, wherein the system further comprises the OS, and a networking interface operatively coupled to the BIOS [Figure 3].

As per claim 28, Westerinen discloses:

An article of manufacture comprising:

a storage medium [Figure 4, reference 17]; and

a plurality of programming instructions stored therein , designed to enable an apparatus to be able to intervene and save a persistent copy of an operational state of the apparatus, before allowing a suspend process initiated in response to an AC failure condition of the apparatus to place the apparatus in a suspended to memory state to complete [para 0024: system state data are stored before going to a suspended to memory state —which can be the S4 state of the ACPI specification (suspended to disk)].

As per claim 29, Westerinen discloses:

The article of claim 28, wherein the programming instructions are designed to perform the intervening and saving of the persistent copy as a basic input/output system (BIOS), to be given control whenever the suspend process is initiated [para 0015: BIOS is programmed to be part of the mechanism for preserving the data state].

As per claim 32, Westerinen discloses:

In an apparatus, a method of operation comprising:

initiating a suspend process to place the apparatus in a suspended to memory state due to a reason other than an AC failure condition of the apparatus [Figure 4 and para 0032: power button pressed send the system in a standby state (suspended to memory)];

intervening and preserving a persistent copy of an operational state of the apparatus [para 0024: before entering hibernation the contents of the RAM and CPU settings (operational state) are transferred to a hard disk];

signaling an AC failure condition of the apparatus [para 0033: when AC fails, ON_BATT signal is assert];

supplying power from a backup power source to the apparatus for at least a time period [Figure 4, reference 100-102: battery supplies power for a while];

completing the preserving of the persistent copy of the operational state of the apparatus [para 0024: before entering hibernation the contents of the RAM and CPU settings (operational state) are transferred to a hard disk];

completing the suspend process and placing the apparatus in the suspended to memory state, sustained by the supplied backup power [Figure 4: system in place in state S3 (suspended to memory) following a power failure and sustained by a battery (reference 96)]; and

immediately waking the apparatus to respond to the AC failure condition [Figure 4, reference 95-98: waking system to respond to power failure].

As per claim 33, Westerinen discloses:

The method of claim 32, wherein the method further comprises initiating a resume process to resume the apparatus from the operational state suspended in memory, initiating another suspend process, and intervening and preserving another persistent copy of an operational state of the apparatus, before completing said another suspend process and placing the apparatus in the suspended to memory state again, sustained by the supplied backup power [Figure 4: once system returns to reference 90 (resume apparatus from the operation state suspended in memory) it is able to repeat the suspend, intervening and preserving, completing and placing again sustained by the supplied backup power].

As per claim 34, Westerinen discloses:

In an apparatus, a method of operation comprising:

initiating a suspend process to place the apparatus in a suspended to memory state due to a reason other than an AC failure condition of the apparatus [Figure 4 and para 0032: power button pressed send the system in a standby state (suspended to memory)];

intervening and preserving a persistent copy of an operational state of the apparatus [para 0024: before entering hibernation the contents of the RAM and CPU settings (operational state) are transferred to a hard disk];

completing the suspend process and placing the apparatus in the suspended to memory state [Figure 4: system in place in state S3 (suspended to memory)];

signaling an AC failure condition of the apparatus [para 0033: when AC fails, ON_BATT signal is assert];

supplying power from a backup power source to the apparatus for at least a time period [Figure 4, reference 100-102: battery supplies power for a while]; and

waking the apparatus to respond to the AC failure condition [Figure 4, reference 96 to reference 98: controller wakes the system when AC fails].

As per claim 35, Westerinen discloses:

The method of claim 34, wherein the method further comprises initiating a resume process to resume the apparatus from the operational state suspended in memory, initiating another suspend process, and intervening and preserving another persistent copy of an operational state of the apparatus, before completing said another suspend process and placing the apparatus in the suspended to memory state again, sustained by the supplied backup power [Figure 4: once system returns to reference 90 (resume apparatus from the operation state suspended in memory) it is able to repeat the suspend, intervening and preserving, completing and placing again sustained by the supplied backup power]..

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Westerinen (United States Patent Publication No. 2004/0088589) as applied to claims 1 above, and further in view of Hsu (United States Patent No. 6,618,813).

As per claim 2, Westerinen discloses:

The method of claim 1, wherein the suspend process is initiated by an operating system (OS) of the apparatus [para 0024], and comprises the OS instructing a controller of the apparatus *to shut off delivery of normal power within the apparatus, leaving only delivery of standby power within the apparatus.*

Westerinen does not explicitly disclose:

to shut off delivery of normal power within the apparatus, leaving only delivery of standby power within the apparatus.

Hsu discloses:

to shut off delivery of normal power within the apparatus, leaving only delivery of standby power within the apparatus [column 6, lines 45-48: main power (normal power) shut off leaving only standby power].

Both Hsu and Westerinen disclose computer systems that are capable of preserving their operational states when there is a power failure. The methods disclosed in both systems include a step where the systems enter the S3 or S4 state. Westerinen does not explicitly disclose shutting off the normal power while Hsu does. Turning off the main power conserves power since only a few components are require to store operating states [column 2, lines 56-69]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the turning off the main power as taught in Hsu into the system of Westerinen to create a computer system that more power efficient when dealing with AC power failure.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Westerinen (United States Patent Publication No. 2004/0088589) as applied to claims 1 above, and further in view of Cheok (United States Patent No. 2004/0073818).

As per claim 3, Westerinen discloses:

The method of claim 2, wherein

the OS instructing comprises the OS attempting to write to a register of the controller; and

the intervening comprises the controller in response to the OS attempted write, causing a basic input/output system (BIOS) to perform the preservation of the operational state of the

apparatus [para 0015: BIOS is programmed to be part of the mechanism for preserving the data state].

Westerinen does not discloses:

the OS instructing comprises the OS attempting to write to a register of the controller; and

Cheok discloses:

the OS instructing comprises the OS attempting to write to a register of the controller [para 0055: OS writes to PM1a register (which is connected to controller)];

Both Westerinen and Cheok disclose systems that function in various power modes according to ACPI standards. Westerinen does not disclose the OS writing to a register of the controller, instead Westerinen discloses the switchover circuits writes to a register of the controller [Westerinen, para 0027]. In Westerinen, the switchover circuit is the component that detects power failure and initiates a move the system to a lower power state. In Cheok, the OS determines whether or not to place the system in a lower power state [Cheok, para 0055]. Having the OS determine the power states of a computer would allow for power management to be platform independent [Cheok, para 0008]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate having the OS write to the register as taught in Cheok into the system of Westerinen to create a computer system that allows for power management to be platform independent.

Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westerinen (United States Patent Publication No. 2004/0088589), and further in view of Mustafa (United States Patent No. 6,243,831).

As per claim 11, Westerinen discloses:

In an apparatus, a method of operation comprising:

commencing a cold start reset process on re-application of AC power to the apparatus while the apparatus is in an un-powered state, [Figure 4, para 0034: cold start reset while system is in off state];

determining as part of the cold start reset process, whether a persistent storage of the apparatus comprises a saved operational state of the apparatus ;

restoring the saved operational state of the apparatus from the persistent storage to a memory of the apparatus, *if the persistent storage is determined to have a saved operational state of the apparatus* [para 0034: resumes working state using the previously stored state data]; and

continuing the cold start reset process as a resume process to allow the apparatus to start operation in an active state, continuing from the restored operational state of the apparatus [para 0034: resumes working state using the previously stored state data].

Westerinen does not explicitly disclose:

determining as part of the cold start reset process, whether a persistent storage of the apparatus comprises a saved operational state of the apparatus ;

if the persistent storage is determined to have a saved operational state of the apparatus

Mustafa discloses:

determining as part of the cold start reset process, whether a persistent storage of the apparatus comprises a saved operational state of the apparatus [column 8, lines 15-23 and Figure 4: checks CMOS bit to determine if states were saved to nvm];

Mustafa and Westerinen both disclose power loss protection systems. While Westerinen does not explicitly disclose checking if persistent storage has saved states, Mustafa does. Checking for saved states as part of a cold start reset process is well known in the art and allows for the system to handle cases where the state of the system was not properly saved. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the checking of saved states as taught in Mustafa into the system of Westerinen to create a computer system that is able to handle instances when the system state is not saved during a power loss.

As per claim 12, Westerinen discloses:

The method of claim 11, wherein the determining and restoring are performed by a basic input/output system (BIOS) of the apparatus [para 0024: BIOS restores state of the system]; and

the continuing of the cold start reset process as a resume process comprises the BIOS transferring control to an operating system (OS) of the apparatus to complete the resume process and operate the apparatus in the active state, starting from the restored operational state in memory [para 0024: BIOS resumes same condition of system before hibernation and passes

control to the OS after initialization (as per para 0015)]

As per claim 13, Mustafa discloses:

The method of claim 11, wherein the method further comprises continuing with the cold start reset process, upon determining the persistent storage not comprising a saved operational state of the apparatus [column 8, lines 15-23 and Figure 4: checks CMOS bit to determine if states were saved to nvm. If it is not set, it continues with reset process].

Mustafa and Westerinen both disclose power loss protection systems. While Westerinen does not explicitly disclose continuing reset process after determining there are no saved states, Mustafa does. Having the system continue with the reset process if there are no saved states is well known in the art and allows for the system to handle cases where the state of the system was not properly saved. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the checking of saved states as taught in Mustafa into the system of Westerinen to create a computer system that is able to handle instances when the system state is not saved during a power loss.

Claims 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westerinen (United States Patent Publication No. 2004/0088589), and further in view of Cheok (United States Patent No. 2004/0073818).

As per claim 15, Westerinen discloses:

The system of claim 14, wherein

the system further comprises a processor and the OS [Figure 1, reference 14 and 22]; and

the controller *comprises a register to which the OS writes to initiate the suspend process to place the system in the suspended to memory state , and the* controller is equipped to cause the BIOS to gain control, to enable the BIOS to intervene [para 0015: BIOS involved with preserving state data], *in response to an attempted write to the register by the OS.*

Westerinen does not disclose:

comprises a register to which the OS writes to initiate the suspend process to place the system in the suspended to memory state , ..., in response to an attempted write to the register by the OS

Cheok discloses:

comprises a register to which the OS writes to initiate the suspend process to place the system in the suspended to memory state [para 0055: OS writes to PM1a register (which is connected to controller) to initiate suspend process to place the system in suspended to memory state (S3)], ..., *in response to an attempted write to the register by the OS*

Both Westerinen and Cheok disclose systems that function in various power modes according to ACPI standards. Westerinen does not disclose the OS writing to a register of the controller, instead Westerinen discloses the switchover circuits writes to a register of the controller [Westerinen, para 0027]. In Westerinen, the switchover circuit is the component that detects power failure and initiates a move to a lower power state. In Cheok, the OS determines whether or not to place the system in a lower power state [Cheok, para 0055]. Having the OS

determine the power states of a computer would allow for power management to be platform independent [Cheok, para 0008]. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate having the OS write to the register as taught in Cheok into the system of Westerinen to create a computer system that allows for power management to be platform independent.

Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westerinen (United States Patent Publication No. 2004/0088589), and further in view of Mustafa (United States Patent No. 6,243,831).

As per claim 24, Westerinen discloses:

A system comprising:

a memory [Figure 3, reference 17: ram];

a persistent storage to store at least a saved operational state of the system [figure 3, reference 23]; and

a basic I/O system (BIOS) operationally coupled to the memory and the persistent storage to determine, as part of a cold start reset process commenced in response to re-application of AC power to the system while the system is in an un-powered state, *whether the persistent storage comprises a saved operational state of the system,* and to restore the saved operational state of the system from the persistent storage to the memory upon determining existence of the saved operational state of the system in the persistent storage [para 0024, BIOS reads contents and restores state].

Westerinen does not explicitly disclose:

whether the persistent storage comprises a saved operational state of the system,

Mustafa discloses:

whether the persistent storage comprises a saved operational state of the system [column 8, lines 15-23 and Figure 4: checks CMOS bit to determine if states were saved to nvm]

Mustafa and Westerinen both disclose power loss protection systems. While Westerinen does not explicitly disclose checking if persistent storage has saved states, Mustafa does. Checking for saved states as part of a cold start reset process is well known in the art and allows for the system to handle cases where the state of the system was not properly saved. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the checking of saved states as taught in Mustafa into the system of Westerinen to create a computer system that is able to handle instances when the system state is not saved during a power loss.

As per claim 25, Westerinen discloses:

The system of claim 24, wherein the BIOS is further equipped to continue the cold start reset process as a resume process, on determining and restoring the saved operational state of the system from the persistent storage to the memory, to transition the system from the un-powered state to an active state, where the system continues operation, starting from the restored operational state [para 0024: BIOS reads contents and restores state].

As per claim 26, Westerinen discloses:

The system of claim 25, wherein

the system further comprises an operating system [Figure 4, reference 22]; and the BIOS is further designed to transfer control to the operating system to continue and complete the resume process, and resume operating the system at the active state, starting from the restored operating state of the system [para 0024: BIOS resumes same condition of system before hibernation and passes control to the OS after initialization (as per para 0015)].

As per claim 27, Mustafa discloses:

The system of claim 24, wherein the BIOS is further designed to continue the cold start reset process, upon determining the persistent storage not comprising a saved operational state of the system [column 8, lines 15-23 and Figure 4: checks CMOS bit to determine if states were saved to nvm. If it is not set, it continues with reset process].

Mustafa and Westerinen both disclose power loss protection systems. While Westerinen does not explicitly disclose continuing reset process after determining there are no saved states, Mustafa does. Having the system continue with the reset process if there are no saved states is well known in the art and allows for the system to handle cases where the state of the system was not properly saved. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the checking of saved states as taught in Mustafa into the system of Westerinen to create a computer system that is able to handle instances when the system state is not saved during a power loss.

Claims 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westerinen (United States Patent Publication No. 2004/0088589), and further in view of Mustafa (United States Patent No. 6,243,831).

As per claim 30, Westerinen discloses:

An article of manufacture comprising:

a storage medium [Figure 3];

a plurality of programming instructions stored therein, designed to enable an apparatus to

determine as part of a cold start reset process of the apparatus initiated in response to re-application of AC to the apparatus while the apparatus is in an un-powered state [Figure 4, para 0034: cold start reset while system is in off state], *whether a persistent storage of the apparatus comprises a saved operational state of the apparatus,*

restore the saved operational state of the apparatus from the persistent storage to a memory of the apparatus [para 0034]; and

causing the cold start reset process to be completed as a resume process to resume operation of the apparatus in an active state, starting from the restored operational state [para 0034].

Westerinen does not explicitly disclose:

whether a persistent storage of the apparatus comprises a saved operational state of the apparatus,

Mustafa discloses:

whether a persistent storage of the apparatus comprises a saved operational state of the apparatus [column 8, lines 15-23 and Figure 4: checks CMOS bit to determine if states were saved to nvm];

Mustafa and Westerinen both disclose power loss protection systems. While Westerinen does not explicitly disclose checking if persistent storage has saved states, Mustafa does. Checking for saved states as part of a cold start reset process is well known in the art and allows for the system to handle cases where the state of the system was not properly saved. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the checking of saved states as taught in Mustafa into the system of Westerinen to create a computer system that is able to handle instances when the system state is not saved during a power loss.

As per claim 31, Mustafa discloses:

The article of claim 30, wherein the programming instructions are further designed to enable the apparatus to continue and complete the cold start and reset process, after the persistent storage is determined not to comprise a saved operational state of the apparatus [column 8, lines 15-23 and Figure 4: checks CMOS bit to determine if states were saved to nvm. If it is not set, it continues with reset process].

Mustafa and Westerinen both disclose power loss protection systems. While Westerinen does not explicitly disclose continuing reset process after determining there are no saved states, Mustafa does. Having the system continue with the reset process if there are no saved states is well known in the art and allows for the system to handle cases where the state of the system was not properly saved. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the checking of saved states as taught in Mustafa into the system of Westerinen to create a computer system that is able to handle instances when the system state is not saved during a power loss.

Allowable Subject Matter

Claim 5 is objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all the limitations in their respective base claims and any intervening claims. Claims 1 & 5 are indicated allowable as a whole, and further modifications to the scope of the claimed subject matter may jeopardize this indication of allowable subject matter. The claims will be listed below and italicized segments indicate subject matter which over come prior arts.

As per claim 5:

The method of claim 1, wherein the method further comprises *receiving an interruption interrupting the preserving of the persistent copy, in response, aborting the preserving, and* completing the suspend process, placing the apparatus in the suspended to memory state, sustained by the supplied backup power.

The process of receiving an interrupt and aborting the preservation while completing the suspend process overcomes prior arts. There are numerous arts that are similar but do not explicitly express this limitation. Also, the examiner is unable to find sufficient motivation for incorporating these similar arts together. In Crump (United States Patent No. 5,551,043), the interruption of preserving a state (checkpointing) and aborting the preservation are disclosed, however, Crump does not discloses the interrupting and aborting events occurring during a suspend process. Instead, Crump discloses them being ignored [column 6, lines 6-12] while in a suspend process. Other prior art such as Cheok and Westerinen do not explicitly detail the process of receiving an interruption and aborting the preservation. They do imply when an interrupt occurs, the process of preservation is continued. Thus claim 5 is allowable matter with the base/intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack W. Szeto whose telephone number is (571) 272-1537. The examiner can normally be reached on M-F 8 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jws

Bryce P. Bonzo

BRYCE P. BONZO
PRIMARY EXAMINER